

IN THE CLAIMS

Applicant below submits a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please amend claims 1, 8, 13, 16, 18, 22, 28, 30, 33, 34, 36-39 and 40 as shown.
Please cancel claims 7 and 21 without prejudice or disclaimer are amended.

CLAIMS

1. (Currently amended) An analog-to-digital converter comprising:
 a first section having a multi-bit analog to digital converter for receiving an analog input signal and generating an m-bit digital signal[[:]] , and
 an m-bit to n-bit converter (where $m > n$) for receiving the m-bit digital signal and for generating an n-bit digital output signal for outputting across an interface, wherein the m-bit to n-bit converter quantizes the m-bit signal to a lower resolution; and
 a second section having processing means which is arranged to receive the n-bit digital signal and to process the received signal to generate an output digital signal.
2. (Original) An analog-to-digital converter according to claim 1 wherein the multi-bit analog to digital converter is a multi-bit sigma-delta modulator.
3. (Original) An analog-to-digital converter according to claim 1 wherein the m-bit to n-bit converter is an m-bit to single-bit converter.
4. (Original) An analog-to-digital converter according to claim 1 wherein the m-bit to n-bit converter receives the m-bit digital signal at substantially the same rate as it outputs the n-bit digital signal.

5. (Original) An analog-to-digital converter according to claim 1 wherein the m-bit to n-bit converter is a noise-shaping converter.
6. (Original) An analog-to-digital converter according to claim 5 wherein the m-bit to n-bit converter is a digital sigma-delta modulator.
7. Cancelled
8. (Currently amended) An analog-to-digital converter according to claim [[7]] 1 wherein the processing means comprises an n-bit to p-bit converter for receiving the n-bit digital signal from the interface and for generating a p-bit digital signal, where $n < p$ ~~($n < p$) at a higher resolution~~; and
filtering means for filtering the p-bit signal to generate a digital output.
9. (Original) An analog-to-digital converter according to claim 8 wherein the n-bit to p-bit converter is a single-bit to p-bit converter.
10. (Original) An analog-to-digital converter according to claim 8 wherein the n-bit to p-bit converter receives the n-bit digital signal at substantially the same rate as it outputs the p-bit digital signal.
11. (Original) An analog-to-digital converter according to claim 8 wherein $m=p$.
12. (Original) An analog-to-digital converter according to claim 8 wherein the filtering means comprises a decimator.
13. (Currently amended) An analog-to-digital converter according to claim [[7]] 1 wherein the first section is located on a first integrated circuit and the second section is located on a second integrated circuit.

14. (Original) An analog-to-digital converter according to claim 13 wherein the first integrated circuit and second integrated circuit are separately packaged.
15. (Original) An analog-to-digital converter according to claim 13 wherein the first and second integrated circuits are housed within a common package.
16. (Original) An analog-to-digital converter according to claim 7 wherein the second section is formed using a manufacturing geometry which is different than the first section.
17. (Original) An analog-to-digital converter according to claim 16 wherein the second section is formed using a manufacturing geometry which is finer than the first section.
18. (Currently amended) A digital-to-analog converter comprising:
 a first section having an input for receiving an s-bit digital signal from an interface and for generating a t-bit digital signal, where $s < t$, (where $s < t$) at a higher resolution; and
 digital-to-analog conversion means for receiving the t-bit digital signal and generating an analog output; and
 a second section connectable to said first section by said interface and having an input for receiving a digital signal; and,
 processing means for receiving the digital input signal and generating an s-bit digital output signal.
19. (Original) A digital-to-analog converter according to claim 18 wherein the s-bit to t-bit converter receives the s-bit digital signal at substantially the same rate as it outputs the t-bit digital signal.
20. (Original) A digital-to-analog converter according to claim 18 wherein the s-bit to t-bit converter is a single-bit to t-bit converter.
21. Cancelled

22. (Currently amended) A digital-to-analog converter according to claim [[21]] 18 wherein the processing means comprises:

means for generating an r-bit digital signal; and,

an r-bit to s-bit converter (where $r > s$) for receiving the r-bit digital signal and for generating an s-bit output signal for outputting across the interface, the converter thus quantizing the r-bit signal to a lower resolution.

23. (Original) A digital-to-analog converter according to claim 22 wherein the r-bit to s-bit converter is an r-bit to single-bit converter.

24. (Original) A digital-to-analog converter according to claim 22 wherein the r-bit to s-bit converter receives the r-bit signal at substantially the same rate as it outputs the s-bit signal.

25. (Original) A digital-to-analog converter according to claim 22 wherein the r-bit to s-bit converter is a noise-shaping converter.

26. (Original) A digital-to-analog converter according to claim 25 wherein the noise-shaping converter is a sigma-delta modulator.

27. (Original) A digital-to-analog converter according to claim 22 wherein the processing means comprises a further converter for receiving a multi-bit digital signal and for generating the r-bit digital signal.

28. (Currently amended) A digital-to-analog converter according to claim [[21]] 18 wherein the processing means comprises an interpolation ~~filtering~~ filter.

29. (Original) A digital-to-analog converter according to claim 22 wherein $r=t$.

30. (Currently amended) A digital-to-analog converter according to claim ~~[[21]]~~ 18 wherein the ~~first~~ second section is located on a first integrated circuit and the ~~second~~ first section is located on a second integrated circuit.
31. (Original) A digital-to-analog converter according to claim 30 wherein the first integrated circuit and second integrated circuit are separately packaged.
32. (Original) A digital-to-analog converter according to claim 30 wherein the first integrated circuit and second integrated circuit are housed within a common package.
33. (Currently amended) A digital-to-analog converter according to claim ~~[[21]]~~ 18 wherein the ~~second~~ first section is formed using a manufacturing geometry which is different ~~to~~ than that used for the ~~first~~ second section.
34. (Currently amended) A digital-to-analog converter according to claim 33 wherein the ~~second~~ first section is formed using a manufacturing geometry which is coarser than the first section.
35. (Original) Signal processing apparatus in the form of an integrated circuit which comprises the analog-to-digital converter of claim 1 and the digital-to-analog converter of claim 18.
36. (Currently amended) ~~Signal processing apparatus for use as an output stage of an~~ An analog-to-digital converter according to claim 1, further including apparatus comprising an output stage thereof, the apparatus comprising:
- an input for receiving an n-bit signal from ~~the~~ said analog-to-digital converter ~~of claim 1~~,
 - ~~processing means for converting a processor which converts~~ a processor which converts the n-bit digital signal into a p-bit digital signal, where $n < p$ ~~(where $n < p$)~~ at a higher resolution; and

~~filtering means for filtering~~ a filter arranged to receive the p-bit signal to and generate a digital output therefrom.

37. (Currently amended) ~~Signal processing apparatus for use as an input stage of a~~ A digital-to-analog converter according to claim 18, further including apparatus comprising an input stage thereof, the apparatus comprising:

a converter for converting an r-bit digital signal to an s-bit digital signal (where $r > s$) ~~for outputting across an interface to the digital-to-analog converter of claim 18, the converter quantizing the r-bit signal to a lower resolution~~ which is output to said interface.

38. (Currently amended) Signal processing apparatus in the form of an integrated circuit which comprises the converter processing apparatus of claim 36 and the converter processing apparatus of claim 37.

39. (Currently amended) A method of processing an analog signal to generate a digital signal comprising the ~~steps~~ acts of:

receiving an analog input signal and generating an m-bit digital signal in a multi-bit analog-to-digital converter; ~~and,~~

converting the m-bit digital signal into an n-bit digital output signal (where $m > n$) for outputting across an interface, wherein the converting quantizes the m-bit signal to a lower resolution; and

receiving the n-bit digital output signal across said interface and processing the received n-bit digital signal to generate an output digital signal.

40. (Currently amended) A method of processing a digital input signal to generate an analog output signal comprising the ~~steps~~ acts of:

in a first section receiving an s-bit digital signal from an interface;

~~converting~~ generating from the s-bit digital signal into a t-bit digital signal (where $s < t$) at a higher resolution[[:]] and,

converting the t-bit digital signal into an analog output signal; and

in a second section, at an input, receiving a digital input signal, and processing the digital input signal to generate said s-bit digital signal and to deliver said s-bit signal to said interface.

41. (Original) Signal processing apparatus for converting a signal between the analog and digital domains comprising an input section and an output section which are connectable to one another by an interface:

the input section comprising means for converting an input signal into a multi-bit digital format,

an input converter for quantizing the multi-bit signal so as to generate a lower resolution digital signal which can be sent across the interface;

an output converter for converting the lower resolution signal into a higher resolution signal; and

processing means for processing the higher resolution signal to derive an output signal.

42. (Original) Signal processing apparatus according to claim 41 wherein the input converter is a noise-shaping converter.

43. (Original) Signal processing apparatus according to claim 42 wherein the noise-shaping converter is a sigma-delta modulator.

44. (Original) Signal processing apparatus according to claim 41 wherein the lower resolution digital signal is a single-bit signal.